

**Analog-to-Digital Converter Performance Signoff
with Analog FastSPICE™ Transient Noise
at Qualcomm**

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1 Abstract

Analog-to-digital converters (ADCs) are key building blocks in wireless communications and many other applications. Qualcomm pays particular attention to verifying ADC performance in the presence of device noise and to verifying the ADC overall noise performance specifications. Due to limitations in a previous toolset, Qualcomm had to rely on an error-prone manual block-level ADC noise analysis flow that took a long time and required many assumptions. Qualcomm recently adopted a simple ADC noise analysis flow that uses Berkeley Design Automation (BDA) Analog FastSPICE (AFS) transient noise analysis. This capability delivers full-circuit, SPICE-accurate ADC noise analysis—including device noise—in a single simulation run and typically requires less than a day, depending on the complexity of the circuit. The results from the transient noise verification correlate very well to silicon. Qualcomm now uses AFS-based transient noise analysis for ADCs prior to signoff. This white paper highlights ADC noise analysis challenges, describes the previous ADC noise analysis methodology, and details the new signoff methodology.

2 ADC Verification Flow

ADCs are key building blocks in today's RF and mixed-signal integrated circuits. As the level of IC integration grows, these complex circuits need to operate in increasingly hostile on-chip environments. Designers face a wide variety of challenges to verify ADC functionality and performance specifications. Performance requirements vary by end-application and include resolution, dynamic range, linearity, power consumption, speed, bandwidth, and noise immunity. Accurately obtaining key performance metrics before going to silicon is essential.

Designers typically use three major steps to design and verify ADCs:

- Step 1: Design the architecture and determine its system-level performance with MATLAB® or an equivalent system-level tool.
- Step 2: Define block specifications, design the transistor-level blocks, and verify the blocks with "golden" SPICE or RF simulators.
- Step 3: Verify the full ADC at the transistor level with a "golden" SPICE simulator. Post-process the SPICE output to get the key metrics: signal-to-noise ratio (SNR), signal-to-noise-plus-distortion ratio (SNDR), and effective number of bits (ENOB). Optionally, run PVT corners and Monte Carlo for mismatch-sensitive circuits.

These steps are well known, and most IC design teams practice them. Step 3, full transistor-level simulation, is the major challenge. The problem is that traditional simulators do not have sufficient capacity, accuracy, performance, and functionality. Traditional SPICE simulators are accurate but their simulation speed is prohibitive for high over sample ratio delta sigma modulators, where a large number of data points are needed to get good accuracy of the output spectrum. The digital FastSPICE simulators

run significantly faster at the expense of the required accuracy for high-performance analog and RF circuitry.

Adding to the ADC verification challenge, high-performance ADCs require an additional performance signoff step: verifying ADC performance in the presence of device noise. Noise determines the fundamental limits on circuit performance. Noise-related issues are particularly critical in circuits with noise-sensitive architectures, tight specifications, low voltage levels, and high frequencies. This is especially true for circuits implemented in bulk CMOS processes. As designers integrate ADCs in nanometer-scale designs, they also need to measure and optimize for random device noise impact, especially for low-noise applications.

Device noise analysis is even more challenging in ADC architectures in which designers cannot use RF noise analysis techniques (e.g., periodic steady state and periodic noise) at the full-circuit level. Without a direct full-circuit measurement method, designers have had to develop time-intensive, error-prone approximate methods that require significant designer expertise.

Qualcomm developed and previously used a device noise estimation methodology that required breaking down ADCs into sub-blocks, using standard RF analysis to estimate device noise for each, and then manually combining the results. Qualcomm now has added another step to the ADC noise signoff methodology based on full-circuit AFS transient noise analysis. The new methodology is much simpler: add two noise analysis parameters to the standard transient simulation, and then use the same post-processing scripts that are used for the standard transient simulations. The AFS-based methodology is SPICE-accurate, fast, easy, and robust.

The remainder of this paper will focus on sigma-delta ADC noise analysis at Qualcomm, illustrating the difference between the previous block-level approach and the new AFS transient noise based signoff methodology.

3 Sigma-Delta ADC Noise Analysis

Sigma-delta ADC noise analysis is very difficult, because the circuit is non-periodic and has stringent noise requirements. Standard RF periodic noise simulation approaches are not applicable to full-circuit ADCs, because they are non-periodic. Conventional approaches for full-circuit ADC noise analysis requires an experienced designer; tedious effort to ensure block-level PSS/pnoise convergence; risky assumptions and approximations; and a user-intensive, lengthy, and multi-step process.

The block-level methodology Qualcomm originally developed based on periodic noise analysis required the designers to break the ADC into blocks that can be treated as periodic, use standard RF analysis on each, and manually combine the results to obtain an overall noise estimate. This was done because at the time there was no tool that could perform device noise analysis of a full-circuit ADC including random device noise. This is exactly what AFS transient noise analysis provides today.

Block-level approaches are analogous to building a high-performance race car and having to race it without a test drive. One is forced to performance-test each component separately based on your engineering expertise, racetrack experience, assumptions about conditions, etc.—all in a limited time. Then one assembles all of the pieces, puts the car on the track hoping not to have missed anything, and not to have made any bad assumptions. The true performance gets measured for the first time on the first lap. Obviously any race team that could take test drives and adjust their car prior to the race would have an enormous advantage. This scenario is equivalent to going to silicon without verifying full-circuit ADCs with device noise. The true ADC performance can only be validated when first silicon is available.

AFS transient noise analysis enables the equivalent of taking test drives before going to silicon. This has been validated on production designs with very good correlation between lab data and simulations.

4 Sigma-Delta ADC Noise Sources

This section describes the major noise sources in a representative second-order sigma-delta ADC. Second-order sigma-delta ADCs are comprised of two integrators, summers, a quantizer, and a DAC that includes a voltage reference. Figure 1 shows the breakdown of noise referred to the input. Starting with the integrators, the noise referred to each integrator input is n_1 , n_2 . The summer includes noise of n_s before the quantizer. The quantization error is e_q . Finally, n_{ref} is the noise from DAC reference voltage.

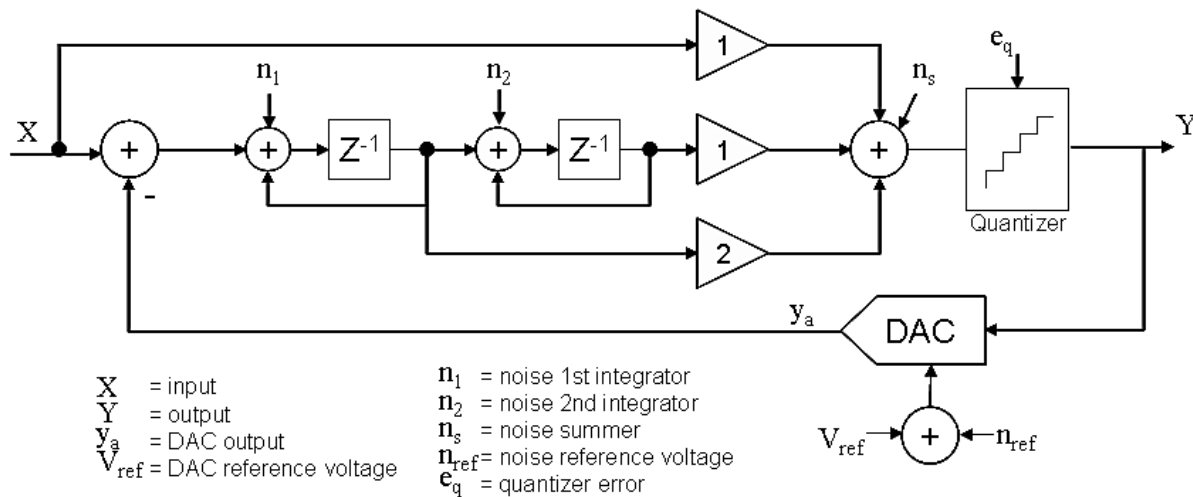


Figure 1. Second-Order Sigma-Delta Modulator

Based on the block diagram the z-domain modulator output and the noise transfer function (NTF) are [1,2]:

$$Y(z) = X(z) + E(z)(1 - z^{-1})^2 \quad (1)$$

$$NTF = (1 - z^{-1})^2 \quad (2)$$

The DAC output voltage y_a can be expressed in terms of its desired signal and error component as follows:

$$y_a = \underbrace{V_{ref}(X + NTF.e_q)}_{\text{Desired}} + \underbrace{n_{ref}(X + NTF.e_q)}_{\text{unwanted noise}} \quad (4)$$

Expanding this equation to show the two noise components as follows:

$$y_a = V_{ref}(X + NTF.e_q) + (n_{ref}X + n_{ref}NTF.e_q) \quad (5)$$

The objective is to produce a signal that is as close as possible to the desired signal, which requires minimizing the unwanted noise.

5 Periodic Block-Level ADC Noise Analysis

Analyzing block-level noise with periodic noise analysis is a multi-step, manual methodology that uses traditional RF simulators. One example is the following procedure for block-level noise analysis:

- Step 1: Estimate n_1 and n_2 by running periodic steady state (PSS) analysis and periodic noise (pnoise) analysis on the integrators and assume that the summer noise (n_s) is small enough to be ignored. Analyze the integrators in isolation by connecting them in a feedback loop configuration as shown in Figure 2.

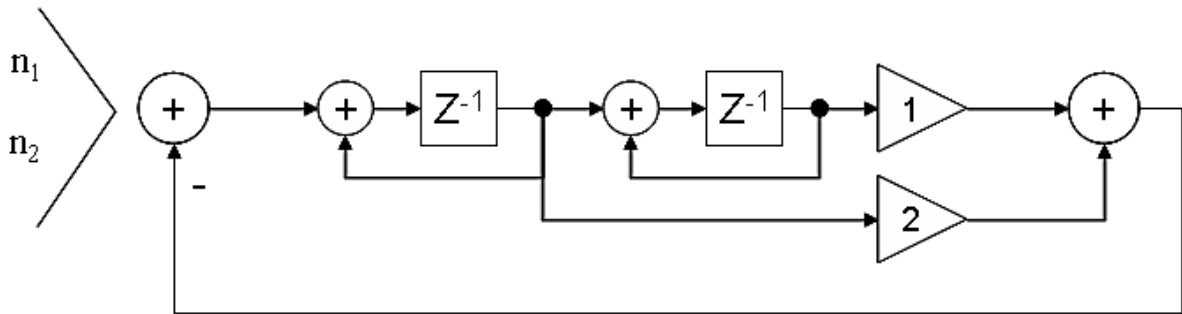


Figure 2. Running PSS/pnoise on Integrators

- Step 2: Estimate n_{ref} by running PSS analysis and pnoise analysis on the DAC modulator output $Y=1$. Use MATLAB to perform convolutions on the two noise error terms in equation (5) above to obtain the input referred noise.
- Step 3: Assume that the quantizer has white noise, i.e., has a flat power spectral density (PSD).
- Step 4: Use a spreadsheet to combine all of the component noise results into an approximate full-circuit noise result.

This methodology requires a designer-intensive verification effort for sigma-delta ADCs. The designer is involved in every step. It is also important to note that this technique requires the designer to make several assumptions based on experience. If any of the assumptions is false or too inaccurate, the noise results will differ significantly from silicon and will likely require a silicon respin. This approach requires expertise in design, RF analysis, ADC noise sources, and process dependencies.

6 Full-Circuit ADC Noise Analysis with AFS Transient Noise

With AFS transient noise analysis there is no need to break up the circuit, the analysis requires minimum designer interaction, and it is silicon-accurate. This full-circuit noise analysis includes random device noise as well as circuit noise such as quantization noise. Transient noise analysis is very intuitive to IC designers. It is simply a transient simulation that includes the random noise for each device at each timestep. The noise magnitude comes from the device noise parameters of the MOS devices, BJTs, and resistors. The result is output waveforms with realistic noise effects. Post-processing the oversampled output waveforms yields the desired noise metrics.

The AFS transient noise analysis use model is the same as standard transient simulation with the addition of two parameters. The tool is fully integrated in the standard design environment and works within the same test beds that Qualcomm uses for transient simulation with traditional SPICE netlists and models.

In order to run transient noise, Qualcomm follows this simple 4-step process:

- Step 1: Determine the simulation time based on the signal and clock frequencies.
- Step 2: Add two frequency parameters to specify the white and flicker noise contribution bandwidths.
- Step 3: Run transient noise analysis with the frequency parameters.
- Step 4: Post-process the output waveforms to determine SNR and other required noise metrics.

This method uses the same ADC noise post-processing as transient simulation. The post-processing uses Fast Fourier Transform techniques to translate the transient noise analysis results from the time domain to the frequency domain, sampling a continuous waveform and computing its PSD. From the PSD one can calculate noise metrics such as SNR, SNDR, and ENOB.

7 Results from AFS Transient Noise Simulation

Qualcomm uses AFS transient noise for diverse ADC architectures and all have shown very good correlation with silicon measurement data. AFS transient noise is key to confirming that nothing was overlooked in the design of each block. Below we present the results and comparisons to transient without noise and silicon measurements for a 4th order sigma-delta ADC.

Table 1 shows the noise voltage and SNDR for AFS transient simulation, AFS transient noise analysis, and the in-band noise voltage from silicon measurement. The AFS transient noise simulation completed in 6.05 hrs and correlates to silicon data by <1.5 dB.

| | Noise Voltage | SNDR |
|------------------------------|---------------|---------|
| AFS Transient Simulation | 79.4 uV | 77.5 dB |
| AFS Transient Noise Analysis | 125.7 uV | 73.5 dB |
| Silicon Measurement | 105.3 uV | 75.0 dB |

Table 1: Noise Voltage and SNDR Results

Figure 3 shows the power spectral density for the ADC simulations. The time-domain results are post-processed to the frequency domain and show only the noise results with the input signal removed. This plot compares the results of AFS transient simulation with AFS transient noise analysis. AFS transient noise accurately predicts that device noise adds ~ 25 dB to the noise floor of the ADC output spectrum as compared to traditional transient simulation that does not include device noise.

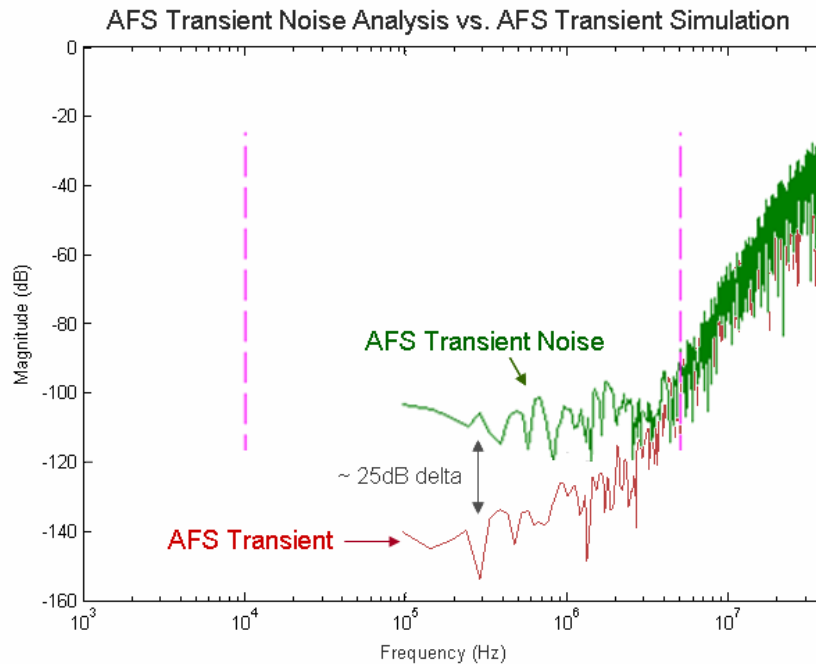


Figure 3. AFS Simulation Results

Figure 4 shows the silicon measurements from the same ADC with 120,000 data points.

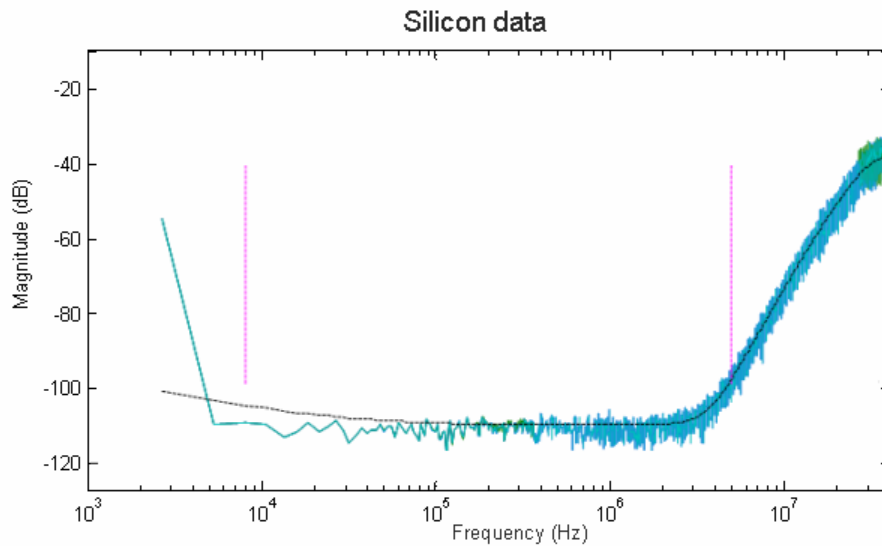


Figure 4. Silicon Measurement Data

Figure 5 shows the results for AFS transient simulation, AFS transient noise analysis, and silicon measurement data. The plot clearly shows the inadequacy of traditional transient simulation and the excellent correlation of AFS transient noise with silicon. AFS transient noise analysis produces accurate results. The silicon data has a smaller point-to-point variance since it is based on a much larger number of data points than the simulation. The accuracy of transient noise versus silicon will further improve if the number of simulation data points is increased.

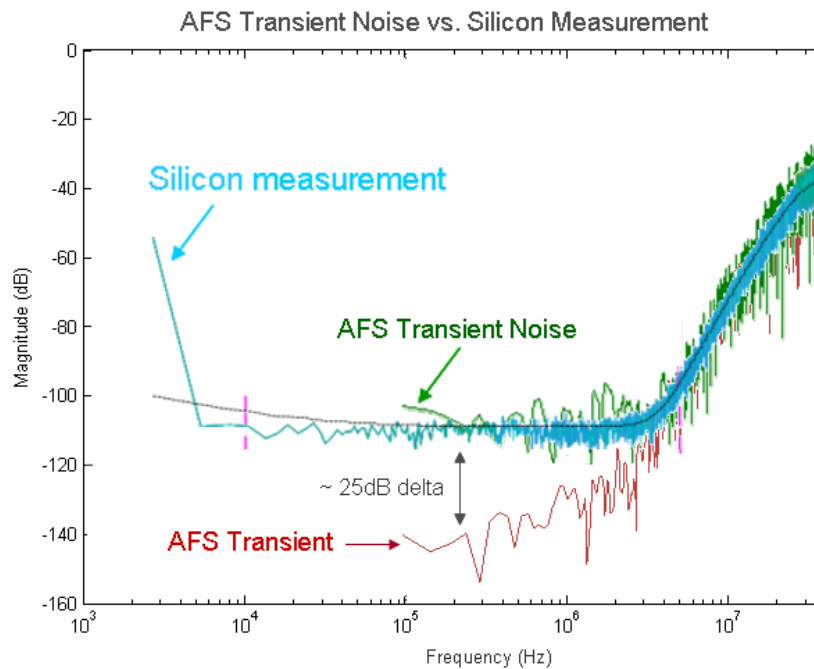


Figure 5. Silicon Measurement and AFS Transient Noise Analysis

8 Conclusion

The Qualcomm ADC design flow now includes the Berkeley Design Automation Analog FastSPICE transient noise analysis as part of design signoff. The AFS transient noise analysis methodology provides silicon-accurate device noise analysis for ADCs. The results also show that traditional transient simulation underestimates the impact of device noise on the noise floor by as much as 25dB. Analog FastSPICE transient noise analysis tremendously improved verification confidence prior to tapeout and Qualcomm now requires AFS transient noise analysis for all ADCs as a design signoff criterion.

9 References

- [1] R. Schreier and G. Temes, "Understanding Delta-Sigma Data Converters", Wiley-IEEE Press, ISBN: 978-0-471-46585-0.
- [2] P.M. Aziz et al, "An Overview of Sigma-Delta Converters," IEEE Signal Processing Magazine, January 1999.

10 About the Authors

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